Software-Programmable Digital Pre-Distortion on New Generation FPGAs

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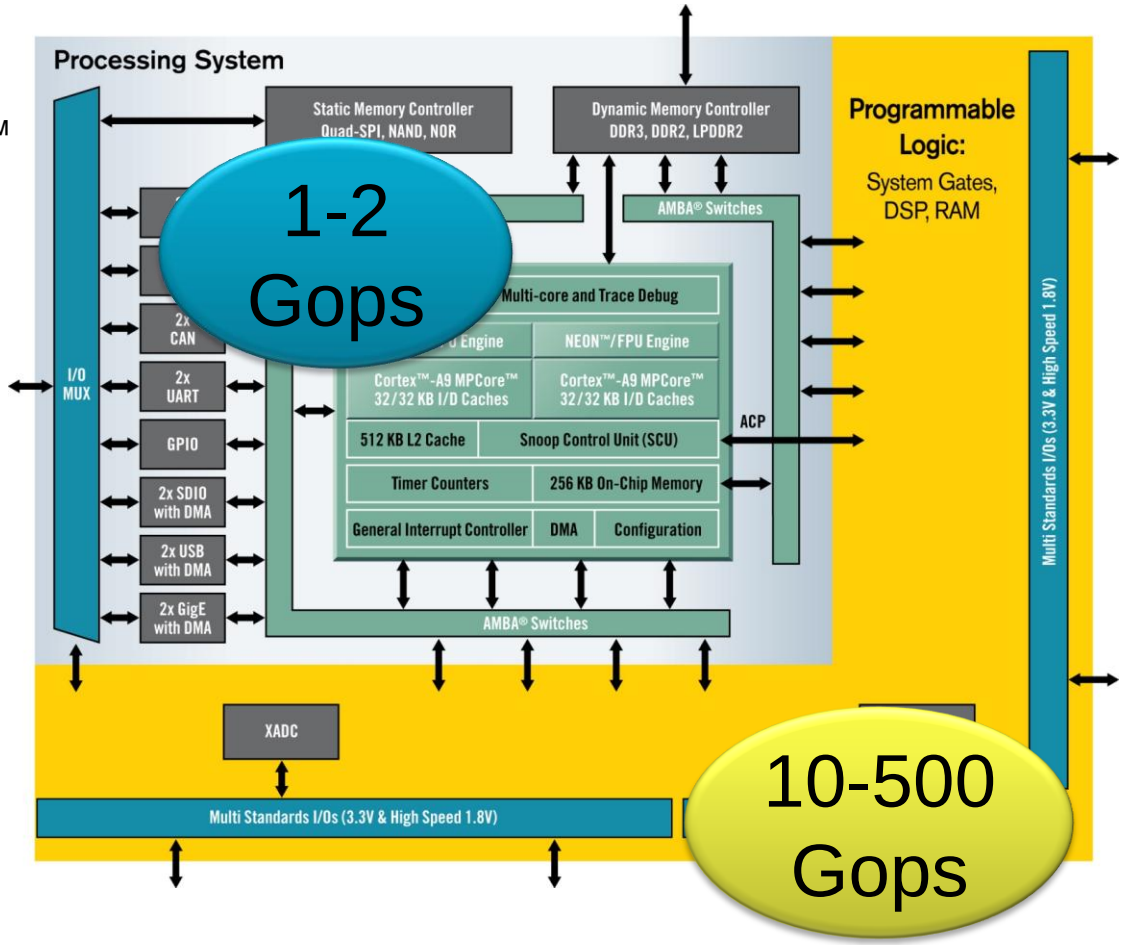
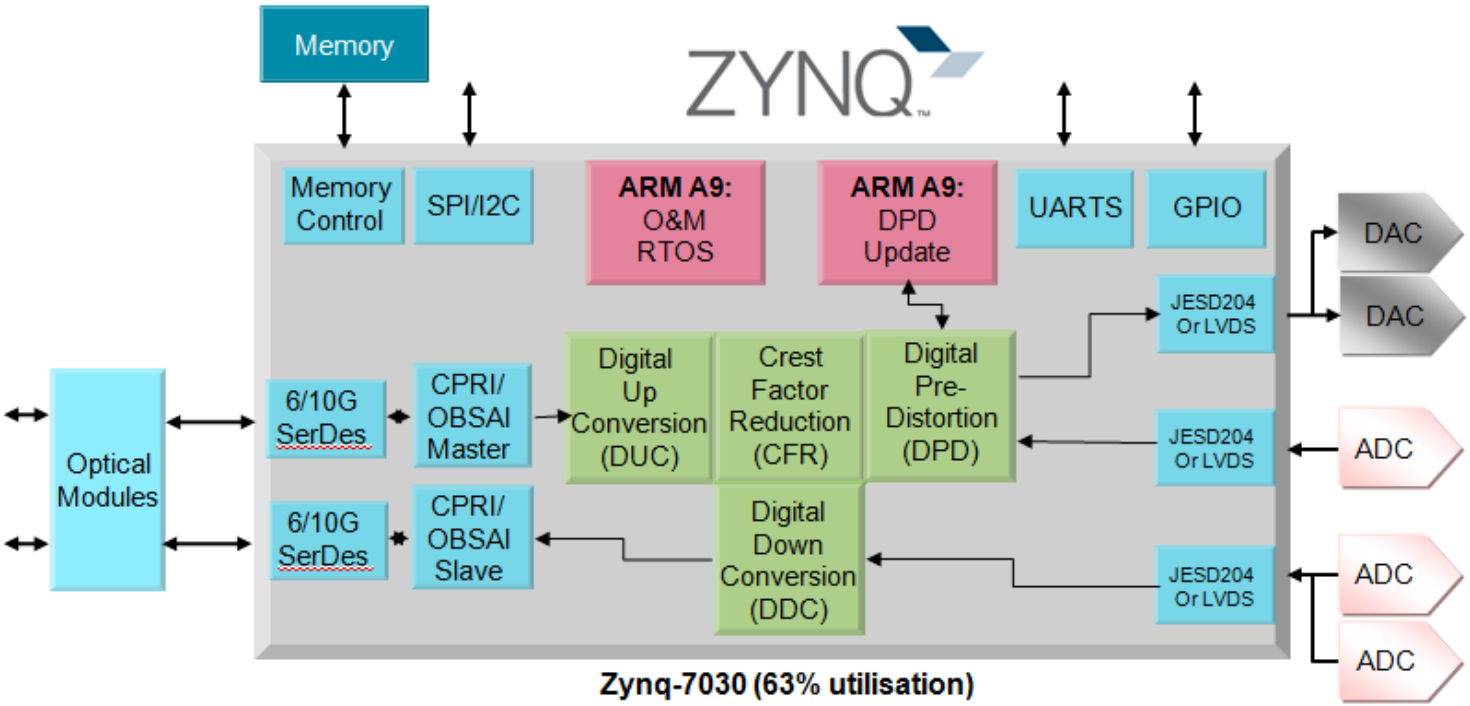
Zynq-7000 Embedded Processing Platform

- **Processor core complex**
  - Two ARM® Cortex™-A9 with NEON™ extensions
  - Floating Point support
  - Up to 1 GHz operation
  - L2 Cache – 512KB Unified
  - On-Chip Memory of 256KB
  - Integrated Memory Controllers
  - Run full Linux
- **State-of-the-art programmable logic**
  - 28K-235K logic cells
  - High bandwidth AMBA interconnect
  - ACP port - cache coherency for additional soft processors



How to Leverage the Compute Power of the Fabric?

How Can Zynq Be Used in Wireless Applications?

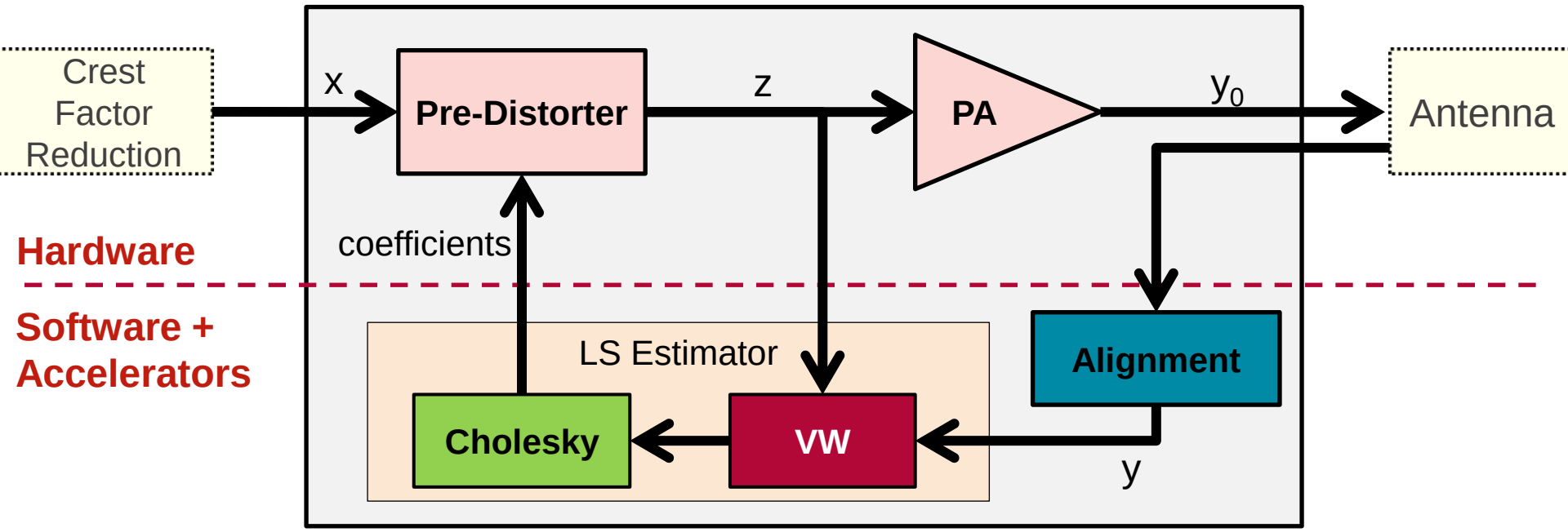


Zynq-7030 (63% utilisation)

- Cost and power reduction by integrated solution
- Performance increase by exploiting the massive compute power of multi-core processors and programmable logic

Zynq: A new paradigm of integration programmed from C/C++

Digital Pre-Distortion Functionality



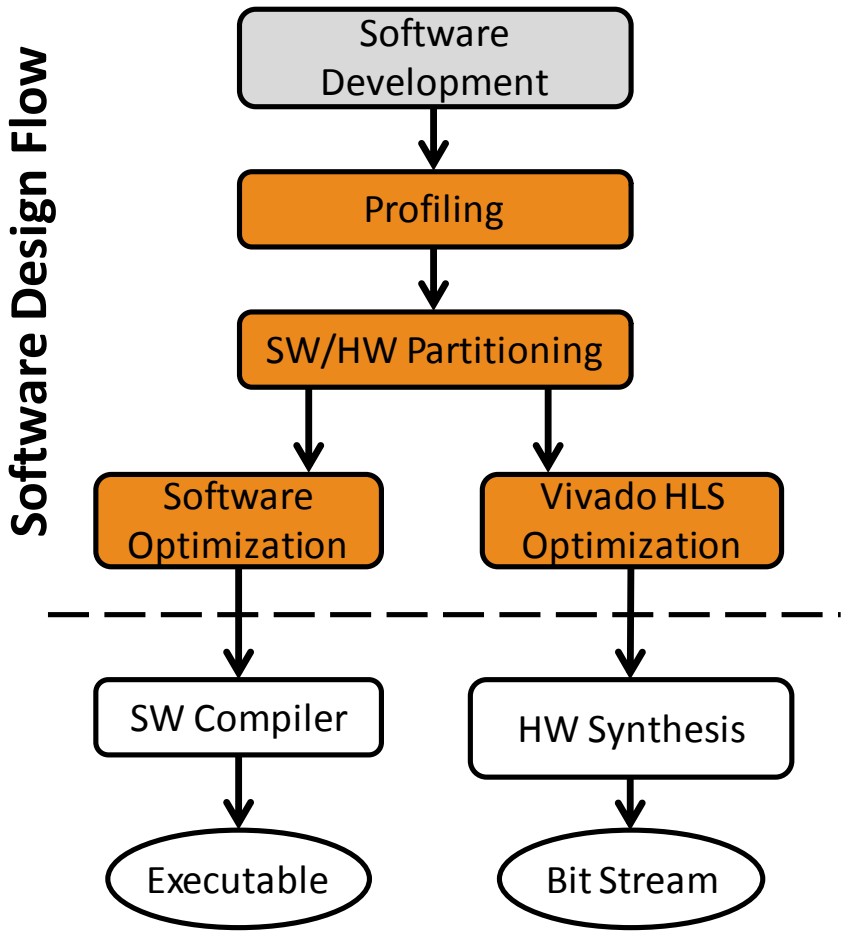
Improve features:

- Support wider bandwidths
- Larger antenna configurations

- **Increase coefficients**
- **Lower run time**
- **Enable SW programmability**

Software Programmable DPD: Allow Custom Algorithm Implementation

Design Flow Overview

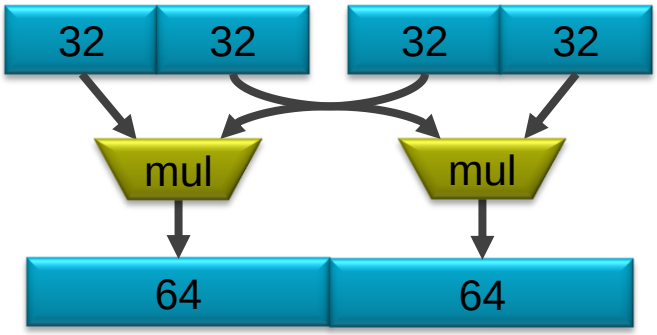


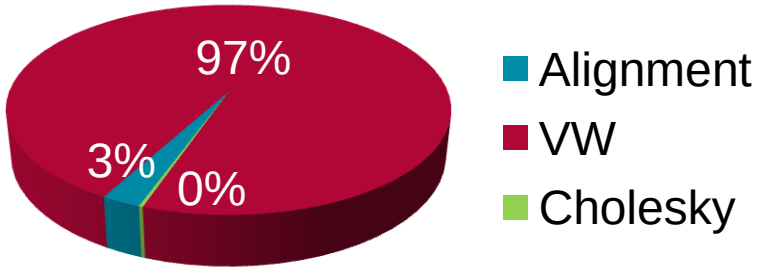
- **Software Profiling**
  - Identify bottlenecks in the SW
- **HW/SW Partitioning**
  - Partition functionality so that processors and accelerators are fully utilized
- **SW Optimization**
  - Exploit SIMD vector unit on Zynq
- **HW Optimization**
  - Offload functionality to Programmable Logic using Vivado HLS

Objective: Program Zynq using a complete C/C++ design flow

Software Profiling and Optimization

- **Initial SW profiling**
  - Several thousand lines of C code
- **Focus on VW functionality**
- **Use of NEON intrinsics (ISA)**
  - Low-level ARM-A9 programming





Target Update Time: 50ms (faster is better)

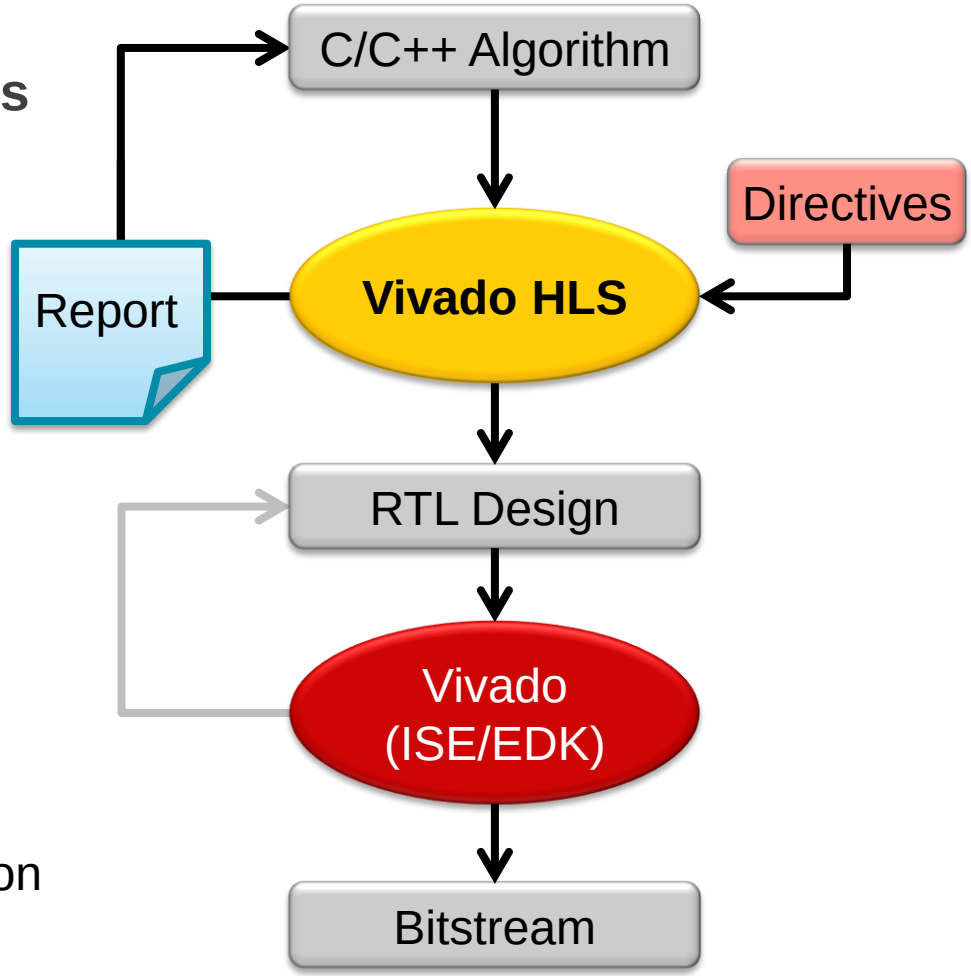
	x86 2GHz	Zynq 800MHz
Original	0.66s	**1.20s**
Optimized	0.22s	**0.54s**
With NEON	n/a	**0.25s**

Speed-up: 5x

Further Improvement Needs Hardware Acceleration

Programming Xilinx FPGA's from C/C++

- **Enables software programmers to target Xilinx FPGAs**
  - Software-programmability
  - Portability: 7-Series, Zynq
- **Delivers productivity increase for RTL designers**
  - C/C++ level verification and testbench reuse
  - Earlier area / latency reports
  - Software-driven design exploration



More Turns Per Day

VW Matrix Computation Using Vivado HLS

```
for (int i = 0; i < NumCoeffs; ++i)
{
#pragma HLS pipeline II=2

  W[i].real +=
      (INT64)u[i].real*tx.real
    + (INT64)u[i].imag*tx.imag;

  W[i].imag +=
      (INT64)u[i].real*tx.imag
    - (INT64)u[i].imag*tx.real;
}
```

+

```
create_clock -period 5
set_part xc7z020clg484-2
```

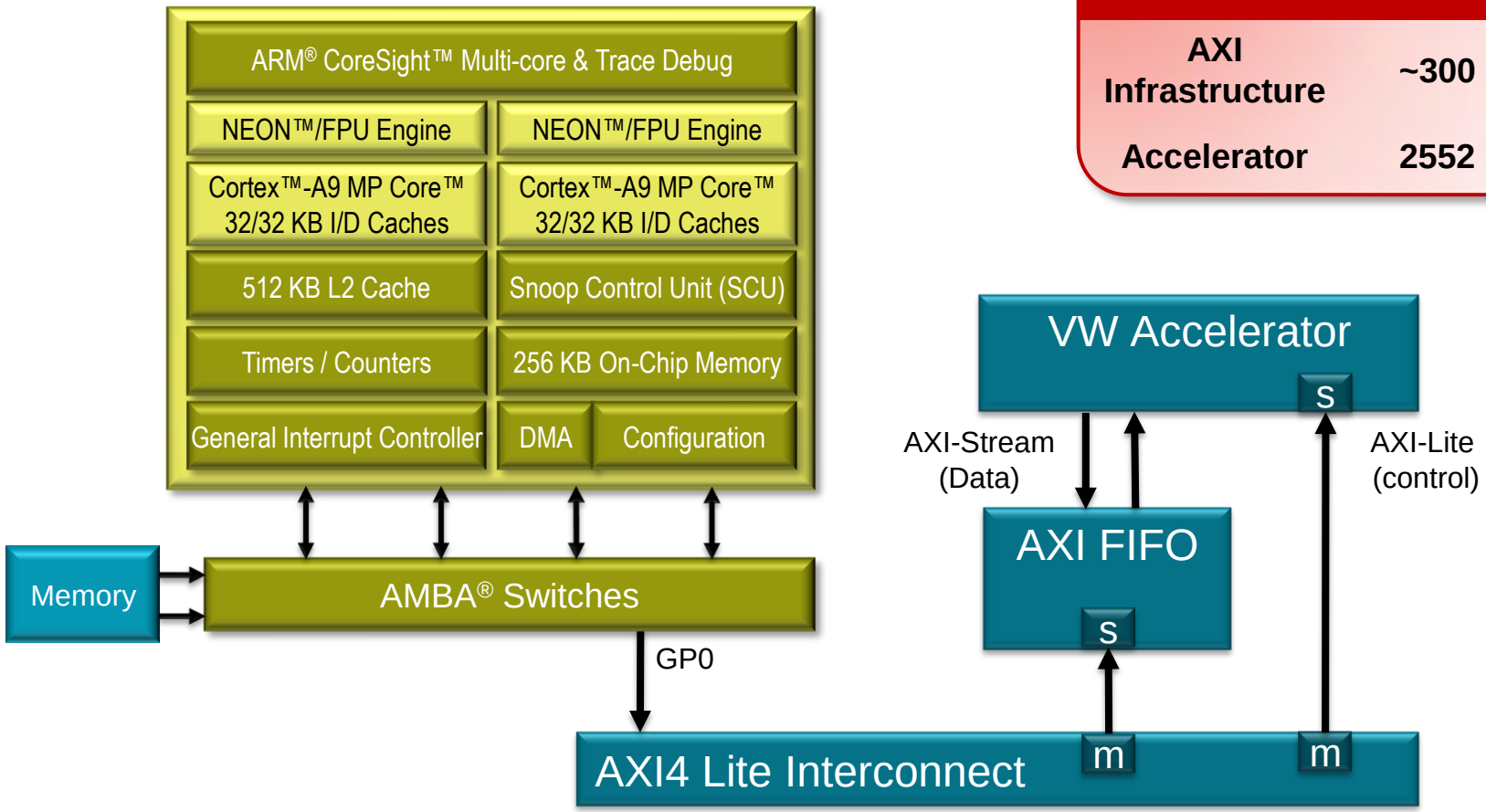
Multipliers: 2
Adders: 2

- **User-driven accelerator optimization based on directives**
  - Enforce resource sharing
  - Insert pipelines
- **Design exploration parameters**
  - Maximum number of coefficients
  - Unroll factors

Accelerator Off-Load to Programmable Logic from C/C++

DPD Architecture on Zynq

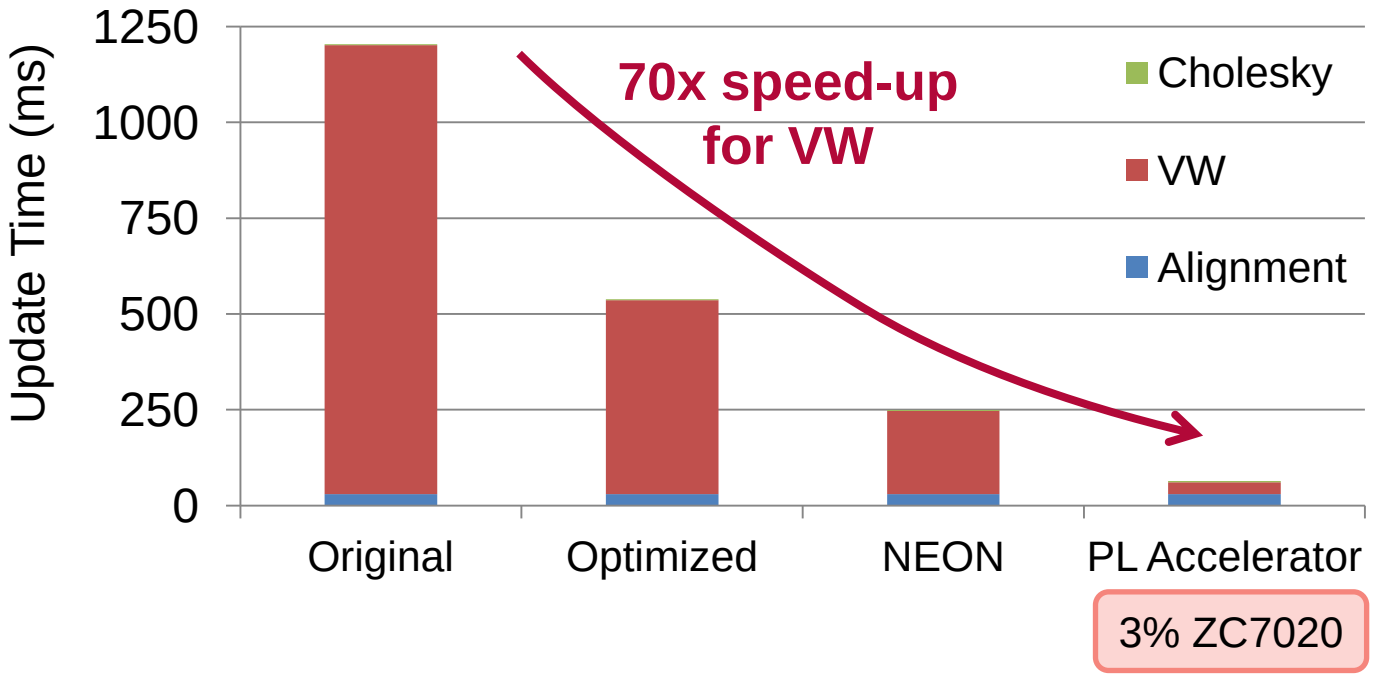
	FF	LUT
AXI Infrastructure	~300	~300
Accelerator	2552	2605



Programmable Logic running @ 250MHz

Reduced Resources – no DMA required

Digital Pre-Distortion on Zynq from C/C++



- **Significant speed-up**
- **Full software programmability**

Zynq + Vivado HLS:
Excellent Match for Challenging Wireless Applications

Software-Programmable DPD: Conclusions

Improved DPD features

- Very competitive full DPD update times
- Support for wider bandwidths and increased number of antennas

Program Zynq using Software approach

- Acceleration using Vivado HLS
- Design productivity increase (verification, design exploration)

DPD system-level partitioning

- Low-complexity: NEON SIMD Unit
- High-complexity: Offload to Programmable Logic